Electronic Version
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Claims

[c1] 1. A method for performing static timing analysis on an integrated circuit design, said method comprising:

performing static timing analysis on a final circuit netlist utilizing a snip file;

converting said snip file to a plurality of cutpoints after said final circuit netlist met all timing constraints under said static timing analysis;

performing formal verification on said plurality of cutpoints;

determining whether or not said plurality of cutpoints pass said formal verification; and

in response to a determination that said plurality of cutpoints do not pass said formal verification, issuing a flag to alert a user.

[c2] 2. The method of Claim 1, wherein said method further includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, modifying said final netlist list and returning to said performing static timing analysis with said modified final circuit netlist.

[c3] 3. The method of Claim 1, wherein said method further

includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, modifying said snip file and returning to said converting said snip file with said modified snip file.

[c4] 4. The method of Claim 1, wherein said method further includes, in response to a determination that said plurality of cutpoints pass said formal verification, sending said final netlist file to manufacturing.

[c5] 5. The method of Claim 1, wherein said performing formal verification further includes performing a functional equivalence comparison between said plurality of cutpoints and corresponding HDL design of said plurality of cutpoints.

[c6] 6. The method of Claim 1, wherein said snip files includes signals and/or timing paths that are not subject to said static timing analysis.

[c7] 7. A computer program product residing on a computer usable medium for performing static timing analysis on an integrated circuit design, said computer program product comprising:

program code means for performing static timing analysis on a final circuit netlist utilizing a snip file;

program code means for converting said snip file to a

plurality of cutpoints after said final circuit netlist met all timing constraints under said static timing analysis;

program code means for performing formal verification on said plurality of cutpoints;

program code means for determining whether or not said plurality of cutpoints pass said formal verification; and

program code means for issuing a flag to alert a user, in response to a determination that said plurality of cutpoints do not pass said formal verification.

[c8] 8. The computer program product of Claim 7, wherein said computer program product further includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, program code means for modifying said final netlist list and returning to said performing static timing analysis with said modified final circuit netlist.

[c9] 9. The computer program product of Claim 7, wherein said computer program product further includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, program code means for modifying said snip file and returning to said converting said snip file with said modified snip file.

[c10] 10. The computer program product of Claim 7, wherein said computer program product further includes, in response to a determination that said plurality of cutpoints pass said formal verification, program code means for sending said final netlist file to manufacturing.

[c11] 11. The computer program product of Claim 7, wherein said computer program product for performing formal verification further includes program code means for performing a functional equivalence comparison between said plurality of cutpoints and corresponding HDL design of said plurality of cutpoints.

[c12] 12. The computer program product of Claim 7, wherein said snip files includes signals and/or timing paths that are not subject to said static timing analysis.

[c13] 13. A computer system for performing static timing analysis on an integrated circuit design, said computer system comprising:

means for performing static timing analysis on a final circuit netlist utilizing a snip file;

means for converting said snip file to a plurality of cutpoints after said final circuit netlist met all timing constraints under said static timing analysis;

means for performing formal verification on said plurality of cutpoints;

means for determining whether or not said plurality of cutpoints pass said formal verification; and means for issuing a flag to alert a user, in response to a determination that said plurality of cutpoints do not pass said formal verification.

[c14] 14. The computer system of Claim 13, wherein said computer system further includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, means for modifying said final netlist list and returning to said performing static timing analysis with said modified final circuit netlist.

[c15] 15. The computer system of Claim 13, wherein said computer system further includes, in response to a determination that said plurality of cutpoints do not pass said formal verification, means for modifying said snip file and returning to said converting said snip file with said modified snip file.

[c16] 16. The computer system of Claim 13, wherein said computer system further includes, in response to a determination that said plurality of cutpoints pass said formal verification, means for sending said final netlist file to manufacturing.

[c17] 17. The computer system of Claim 13, wherein said

computer system for performing formal verification further includes means for performing a functional equivalence comparison between said plurality of cutpoints and corresponding HDL design of said plurality of cutpoints.

[c18] 18. The computer system of Claim 13, wherein said snip files includes signals and/or timing paths that are not subject to said static timing analysis.